Design of Switched Capacitor Based Ring Modulator Using Differential Voltage Current Conveyor and Op-Amp 180-90 nm Technology

N.Prabhakaran ¹, Madhusudhana Reddy Barusu ², S.Krishnakumari ³
¹,²,³ Asst Professor, Department of ECE, Vel Tech High Tech Dr Rangrajan Dr Sakunthala Engineering college, AVADI, INDIA.

Abstract:
In this paper, switched-capacitor based ring modulator using differential voltage current conveyor. This current conveyor is capable of conveying current between two terminals with varying different impedance levels. The advantages of frequency response with wide bandwidth, low voltage operation, very low total harmonic distortion, better CMRR, better linearity, high speed and low power when compared to the conventional circuit. It uses in RF mixers, high-frequency precision rectifiers, instrumentation amplifiers and medical applications such as electrical impedance tomography. It implements using MOS transistors. It requires an only small number of passive components. This topology of modulator gives high-frequency capability with low power consumption. The design realized in 180 nanometres (nm) CMOS design process technology. The 3db frequency of the modulator is in the range of 1 Terahertz. The circuit substitutes an operational amplifier in the conventional design with the differential voltage current conveyor (DVCC) for the implementation. The circuits use a single clock signal which sets and resets the DVCC to avoid the inter-modulation distortion to a higher degree of accuracy. Simulation results obtained using CADENCE tool.

Keywords-DVCC, switched capacitor, ring modulator.

1. Introduction:
The current conveyor, the building block for the analogue signal processing, has the versatility and suitability to realize a wide variety of analogue functions. The DVCC is the extension of CCII and has the advantage of high input impedance at both input terminals over CCII.

Amplitude modulation (AM) is the technique that modulates high-frequency carrier amplitude by a baseband signal of much lower frequency. The amplitude modulation (AM), the double side band suppress carrier (DSBSC), and the signal side band (SSB) are the three common types of AM. The DSBSC make use of a multiplying action between modulating signal and carrier wave. The DSBSC obtains using a ring modulator, which uses a square wave as a carrier. The DVCC is receiving considerable attention as they offer analogue designers some significant advantages over the conventional op-amp. These advantages are as follows:

- Improve AC performance with better linearity.
- Wide bandwidth.
- Relatively High slew rate.
- Reduced supply voltage of integrated circuits.
- The requirement of a smaller number of passive components to perform a specific function.
In this paper, we present a switched capacitor based ring modulator using DVCC. The circuit replaces an operational amplifier in the conventional damped integrator, with DVCC. Simulation results obtained using CADENCE on 180nm technology.

2. Differential Voltage Current Conveyor:

Introduction, by A. Sedra and K. Smith in 1970 [1], the second-generation current conveyor (CCII) proved to be versatile. The analog building blocks use to implement numerous high-frequency signal applications like Filters and oscillator for the design of 180 nm technology. When it comes to utilization of demanding differential or floating inputs like impedance converters and current-mode instrumentation amplifiers, which also require two high input impedance terminals, a single CCII block is no more sufficient. Besides, most of these applications employ Floating elements to minimize the number of used CCII blocks. For this reason and to provide two high input impedance terminals, the differential voltage current conveyor (DVCC) was proposed in 1997 [8] as a four-terminal device with the following properties [Fig.1]:

\[
\begin{bmatrix}
I_{Y1} \\
I_{Y2} \\
V_X \\
I_Z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 \\
0 & 0 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_{y1} \\
V_{y2} \\
I_X \\
V_Z
\end{bmatrix}
\]

The above matrix equations can characterize port relations. While the X terminal voltage follows the voltage difference of terminals Y1 and Y2, a current injected at the X terminal is being replicated to the Z terminal. An ideal DVCC exhibits zero input resistance at terminal X and infinite resistance at both Y terminals as well as the Z terminal. The flow direction of output current follows the input current direction with both currents flowing either into or out of the device. Since the DVCC exhibits two high input impedance terminals, it shows itself suitable for handling differential input signals. Besides, it has the advantage of minimizing the number of floating elements inherent in many CCII applications.

![Fig: 1 Symbol for DVCC.](image)

To overcome this problem and to provide two high input impedance terminals, the differential voltage current conveyor (DVCC) proposes a four-terminal device. The symbol of DVCC shown in Fig.1. The popularity of simple circuit function arises from its broad utility in realizing other circuit functions such as higher-order filters, oscillators, phase equalizers, delay equalizers, etc.

By appropriate speculations of admittances, new circuits which can be used as analogue building blocks can construct using DVCC. The circuit implementation is shown in Fig.2. The course implemented using
eight NMOS transistors and four PMOS transistors. It consists of an input differential stage by a source follower stage.

Fig: 2 Circuit Implementation of DVCC

3. CIRCUIT DESCRIPTION

The circuit uses DVCC as a damped integrator to realize a ring modulator. The proposed ring modulator circuit using DVCC shown in Fig.3. The course uses a carrier clock signal as the clock signal for an integrator. In the circuit when the clock is at zero, the input signal is applied directly to the output filter. During this period the inverter stage (containing DVCC and the two capacitors C1 and C2) is reset and its offset voltage stored for cancellation. The analogue continuous-time filter suppresses the higher-order sidebands. The described ring modulator produces the output similar to the output of the conventional ring modulator using a square wave carrier. This means that its output frequency is equal to the carrier frequency and its output amplitude depends on the baseband amplitude. To obtain this, the carrier clock signal turns ON the switch M14. This will pass the input to the DVCC, which acts on the amplifier with negative gain. The switch M18 is turned ON by the carrier clock, and it gives the DVCC output to the output filter. In this case, if it wants to shift these signals as the upper and lower envelopes of the complete AM signal, two signals have to shift up with an offset higher than \( V_{\text{in}} \) peak. These shiftings are carried out by the use of the fixed voltage \( V_{b} \). The modulation index is controlled by \( V_{b} \). Hence, to avoid the over-modulation, the condition of \( V_{\text{in}} \) peak must be used. Because \( \text{CLK} \) signal turns on M18 in the zero states of the carrier clock (inverter uses to invert the clock to obtain the necessary signal), it directs the input signal \( V_{\text{in}} \) to the filter.

Fig: 3 Switched Capacitor based Ring Modulator using DVCC.
In the switched capacitor the Basic building blocks are capacitors, switches and non-overlapping clocks. In the beside fig Ø1 and Ø2 are not-inverting clocks, MOSFET's are the switches and C1 is the Capacitor.

![Basic Switched Capacitor](image)

**Fig: Basic Switched Capacitor.**

**Calculation of equivalence Resistance:**
The switched capacitor used in the Ring modulator based DVCC is a combination of the M13, M14 and C1 with Vin as the input and the CLK and clkb as the non-overlapping signals.
The equivalent resistance for the switched capacitor used in the design is given by,

\[
\Delta Q_1 = C_1 (V_1 - V_2)
\]

where the \(C_1\) is charged to the \(V_1\) and \(V_2\) during the clock period. 'T' is the clock period (\(f_s = \frac{1}{T}\) (sampling frequency)). Since charge transfer repeated every clock period; we can find the equivalent average due to this charge transfer dividing by the clock period.

\[
I_{avg} = \frac{C_1(V_1 - V_2)}{T}
\]

\[
R_{eq} = \frac{T}{C_1} = \frac{1}{C_1f_s}
\]

Were the \(R_{eq}\) is the equivalence resistance of the switched capacitor.

**Calculation:** capacitance \(C=18\,\text{pF}\) and the clock period is 20k

Then, \(R_{eq} = \frac{1}{\frac{18\,\text{pF}}{20k}} = 2.77\,\text{M}\Omega\).

Thus the equivalence resistance of the switched capacitor is about 2.77M\(\Omega\).

**Sizing:** Were Based on the Transistor sizing the on-resistance and the off resistance of the switches (here MOS devices) decides. The off resistance of the switches can be in the range of the G\(\Omega\), and the on-resistance of the switches can be in the range of the 100\(\Omega\) to 5k\(\Omega\). Used on that the transistor sizing of the switched capacitor Bis did. And to increase the drive capability, the resistance of output MOS is reduced by varying \(W\) and \(L\) of transistors.

<table>
<thead>
<tr>
<th>MOS transistor's</th>
<th>W(nm)</th>
<th>L(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M4</td>
<td>260</td>
<td>180</td>
</tr>
<tr>
<td>M5, M6</td>
<td>240</td>
<td>180</td>
</tr>
<tr>
<td>M7, M8</td>
<td>850</td>
<td>180</td>
</tr>
<tr>
<td>M9, M10</td>
<td>600</td>
<td>180</td>
</tr>
</tbody>
</table>
Table: Aspect Ratios of MOS transistors in Ring Modulator and DVCC

IMPLEMENTATIONS AND RESULTS:

1. DVCC:

Fig: Schematic for differential voltage current conveyor
2. RING MODULATOR USING DVCC

Fig: Schematic for Ring Modulator using DVCC

3. OUTPUT WAVEFORMS:

Fig: Simulated waveforms for Ring modulator, modulating, and carrier(CLK,clkb)signals.
Using the Cadence 180nm technology, the simulation results in accordance obtained for the ring modulator using DVCC (Differential Voltage Current Conveyer). The carrier signal is given as the clock signal (CLK, clkbar(inverting CLK)) and the modulating message is the sinusoidal signal varying from -100mV to 100mV. The transient analysis as done by applying, carrier and the modulating signals are the input signals the resultant ring modulated output is shown in the above figure.

**DC RESPONSE:**

![DC Response of Ring modulator](image1)

**FREQUENCY RESPONSE OR AC ANALYSIS:**

![AC Response for ring modulator circuit](image2)
By using the Cadence Tool, the AC analysis is done, and the frequency response is plotted by having the frequency on the x-axis and the voltage on the Y-axis. The frequency response in the dB also plotted by using the calculator and the waveform obtained in the magnitude. The frequency range of operation of the circuit is above 10T Hz. The 3dB frequency of the design is about 125.9MHz.

**Parameters for the Design:**

The basic principles of switched capacitor circuits can be well understood, assuming ideal opamps. But here Instead of the opamp, DVCC was used. However, some essential nonidealities in the practical switched capacitor are dc gain, unity gain frequency and phase margin, slew rate and dc offset.

**1. DC Gain:**

The circuit to increase the power or amplitude of a signal from the input to the output concerning the transfer function. It defined as the mean ratio of the signal output of a system to the signal input of the same network. It may also be determined on a logarithmic scale, in terms of the decimal logarithm of the same ratio ("dB gain").

\[ Gain = 20 \log_{10} \frac{V_{out}}{V_{in}} \text{ dB} \]

Were the Vout and Vin are the input and the output voltages. The dc gain of intended for switched capacitor circuits is typically on the order of 20 to 40dB. Low dc gains affect the accuracy of the coefficients of the discrete-time transfer function of a switched capacitor filter.

**2. Unity Gain Frequency:**

The unity gain frequency of the op-amp(DVCC) is the maximum bandwidth of the op-amp. This falls with the rising gain.

\[ \text{Bandwidth} = \text{unity gain frequency} / \text{gain} \]

The unity gain frequency and phase margin indicate the small-signal settling behaviour. A general rule of thumb is that the clock frequency of the DVCC(and also opamp) assuming little slew rate behaviour occurs and the phase margin greater than 70 degrees. Modern SC circuits often realized using high-frequency single-stage DVCC(and also opamp) having very large output impedances.

Since loads of this DVCC (and also opamp) are purely capacitive (never resistive), Here that their unity gain frequency and phase margin determined by the load capacitance, which also serves as the compensation capacitor. Thus, in this single-stage DVCC (and also opamp) doubling the load capacitance would halve the unity gain frequency and improve the phase margin.

**3. Slew Rate**

The slew rate defined as the maximum rate of change of the output voltage. Slew rate usually expressed in units of V/µs.

\[ SlewRate = \max\left(\frac{dV_{out}}{dt}\right) \]

where Vout(t) is the output produced by the amplifier as a function of time t. Limitations in slew rate capability can give rise to non-linear effects in amplifiers. The finite slew rate of a DVCC(and also op-amp) can limit the
upper clock rate in switched capacitor circuit as these circuits rely on the charge being quickly transferred from one capacitor to another. Thus, at the instance of charge transfer it is not uncommon for DVCC to slew rate limit.

4. DC Offset:

DC offset is the mean amplitude of the waveform. If the mean amplitude is zero, there is no DC offset. A non-zero dc offset can result in a high output dc offset for the circuit depending on the topology chosen. Fortunately, a technique known as correlated double sampling can significantly reduce this output offset and at the same time reduce low-frequency DVCC input noise (known as 1/f noise).

For calculation of the DC offset the input voltage is kept at zero and the output voltage noted the shift in level is nothing but the DC offset.

Tabulation for the parameters:

The parameters calculated using the waveforms of the design. Were by doing the AC analysis, the frequency response obtained and then by using the waveform and calculator 3dB frequency and bandwidth are calculated. By using the Dc analysis, DC Offset was estimated (by making the input signal zero). By using the transient analysis, the gain (output voltage by input voltage) is determined.

<table>
<thead>
<tr>
<th>SNO</th>
<th>Parameters</th>
<th>Magnitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gain</td>
<td>20dB</td>
</tr>
<tr>
<td>2</td>
<td>Slew Rate</td>
<td>467.16kV/s</td>
</tr>
<tr>
<td>3</td>
<td>CMRR</td>
<td>39.78dB</td>
</tr>
<tr>
<td>4</td>
<td>3dB frequency</td>
<td>125.9MHz</td>
</tr>
<tr>
<td>5</td>
<td>DC Offset</td>
<td>6mV</td>
</tr>
</tbody>
</table>

Table: Parameters of Design

IMPLEMENTATION OF RING MODULATOR USING OPAMP:

CIRCUIT DESCRIPTION:

1. BASIC OPAMP circuit.

Fig: Schematic for primary OPAMP circuit.

2. RING MODULATOR USING OPAMP:

The course uses OPAMP instead of DVCC to realize a ring modulator shown in the figure.
In the circuit when the clock is at zero, the input signal is applied directly to the output filter. During this period the inverter stage (containing opamp and the two capacitors C1 and C2) is reset and its offset voltage stored for cancellation. The analogue continuous-time filter suppresses the higher-order sidebands. The output frequency is equal to the carrier frequency, and its output amplitude depends on the baseband amplitude. To obtain this, the carrier clock signal turns ON the switch M14. This will pass the input to the OPAMP, which acts on the amplifier with negative gain. The switch M18 is turned ON by the carrier clock, and it gives the OPAMP output to the output filter. In this case, if it wants to shift these signals as the upper and lower envelops of the complete AM signal, two signals have to shift up with an offset higher than Vin peak. These shiftings are carried out by the use of the fixed voltage (Vb). Vb controls the modulation index. Hence, to avoid the over-modulation, the condition of Vin peak must be used. Because CLK signal turns on M18 in the zero states of the carrier clock (inverter used to invert the clock to obtain the necessary signal), it directs the input signal (Vin) to the filter. The sizing (W and L) values of the basic OPAMP are as follows, where the length 180nm is constant because the technology file using is 180nm. The first eight transistor’s (M1-M8)are the values of the basic OPAMP, and the M9-M10 is the sizing values of the Ring Modulator using OPAMP. Were the respective values of the sizing shown in the table.

<table>
<thead>
<tr>
<th>MOS transistor's</th>
<th>W(nm)</th>
<th>L(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>220</td>
<td>180</td>
</tr>
<tr>
<td>M1</td>
<td>28</td>
<td>180</td>
</tr>
<tr>
<td>M3-M4</td>
<td>90</td>
<td>180</td>
</tr>
<tr>
<td>M5-M6</td>
<td>25</td>
<td>180</td>
</tr>
<tr>
<td>M7-M8</td>
<td>40</td>
<td>180</td>
</tr>
<tr>
<td>M9, M10</td>
<td>650</td>
<td>180</td>
</tr>
</tbody>
</table>
Table: Aspect Ratios of MOS transistors in Ring Modulator and OPAMP.

Simulation Results:

Vin and Vp are the inputs of the OPAMP, and the output is the output of the OPAMP by having Vdd as 1.8V. The output, we can see that the amplitude of the output doubled to that of the input.

2. AC analysis of ring modulator with OPAMP.

Fig: Simulation results of OPAMP.

Fig: The frequency response.
By using the Cadence Tool, the AC analysis is done, and the frequency response graphs are plotted between the frequency on the x-axis and the voltage on the Y-axis. And the frequency response in the dB is plotted. The 3dB frequency of the design is about 45.71MHz.

3. Ring Modulator output:

![Graph showing ring modulator output](image)

Fig: Ring Modulator using OPAMP.

IMPLEMENTATION OF RING MODULATOR USING DVCC in 90nm:

1. Schematic for ring modulator using DVCC in 90nm

![Schematic for ring modulator using DVCC in 90nm](image)

Fig: Schematic for ring modulator using DVCC in 90nm
2. Simulation results of Ring Modulator using DVCC in 90nm technology.

Fig: Simulation waveform of Ring modulator using DVCC in 90nm.

CONCLUSION

In this paper, a switched capacitor based ring modulator using DVCC in 180nm and 90nm technology has been presented and compared with the ring modulator using OPAMP. The Ring modulator with DVCC has the advantage of excellent frequency response with wide bandwidth, low voltage operation, very low total harmonic distortion, high speed and low power. It can be directly implemented using a MOS transistor, and the circuit can be easily fabricated. The modulator verified through CADENCE simulation. This described ring modulator is suitable for electronic communication applications.

REFERENCES